passing through the encapsulant 24. Moreover, after the encapsulant is formed, the heat sink 23 merely has the first surface 230 thereof bonded to the encapsulant 24, while the side faces 232 and the gold layer 233 coated on the second surface 231 of the heat sink 23 are exposed to the outside of the encapsulant 24. That is, the encapsulant 24 fills a gap between the first surface 230 of the heat sink 23 and the upper surface 200 of the substrate 20. Additionally, while the heat sink 23 has the same surface area as the substrate 20, the exposed surface area of the heat sink 23 can be maximized so as to effectively improve the heat-dissipating efficiency.

On page 9, first paragraph, please amend the paragraph as follows:

Referring finally to FIG. 2(II), the singulated semi-fabricated package 2A is heated for the remaining molding resin 240A on the gold layer 233 to be delaminated from the gold layer 233, due to the difference in thermal expansion coefficient between the molding resin used for forming the encapsulant 24 and the gold layer 233. It is required for the heating to be controlled in the condition of no delamination occurring between the first surface 230 of the heat sink 23 and the encapsulant 24. This allows the remaining molding resin 240A to be easily removed from the gold layer 233 without damaging the bonding of the heat sink 23 to the encapsulant 24. Further, since the remaining molding resin 240A can be completely removed from the gold layer 233, a subsequent deflash process is not necessary, which not only reduces the molding cost but also assures quality of the fabricated semiconductor package 2 (as shown in FIG. 1).

IN THE CLAIMS

Please amend claims 1 and 12 as follows:

1. (Amended) A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

a heat sink having a first surface, a second surface opposing the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the

first surface of the heat sink is attached to the chip for interposing the chip between the chip carrier and the heat sink;

an interface layer formed on the second surface of the heat sink, wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound; and

an encapsulant made of the molding compound for encapsulating the chip and filling a gap between the first surface of the heat sink and the chip carrier, wherein the interface layer and the side surfaces of the heat sink are exposed to outside of the encapsulant, and the side surfaces of the heat sink are in a coplane with side edges of the encapsulant.

12. (Amended) A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

at least one buffer pad attached to the chip and made of a material having a similar thermal expansion coefficient to the chip;

a heat sink having a first surface, a second surface opposing the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface of the heat sink is attached to the buffer pad for interposing the buffer pad between the heat sink and the chip so as to space the first surface from the chip;

an interface layer formed on the second surface of the heat sink, wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound; and

an encapsulant made of the molding compound for encapsulating the chip and the buffer pad, and for filling a gap between the first surface of the heat sink and the chip carrier, wherein the interface layer and the side surfaces of the heat sink are exposed to outside of the encapsulant, and the side surfaces of the heat sink are in a coplane with side edges of the encapsulant.